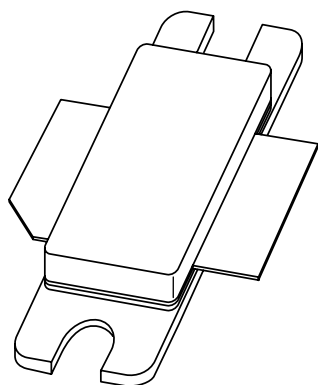


DATA SHEET



BLF1049

Base station LDMOS transistor

Product specification
Supersedes data of 2001 Dec 05

2003 May 14

Base station LDMOS transistor

BLF1049

FEATURES

- Typical performance at a supply voltage of 27 V:
 - 1-tone CW; $I_{DQ} = 1000$ mA
 - Output power = 125 W
 - Gain = 16.5 dB
 - Efficiency = 54%
 - EDGE output power = 45 W (AV)
 - ACPR400 = -64 dBc at 400 kHz (EDGE; $I_{DQ} = 750$ mA)
 - EVM = 2% rms (AV) (EDGE; $I_{DQ} = 750$ mA)
- Easy power control
- Excellent ruggedness
- High power gain
- Excellent thermal stability
- Designed for broadband operation (800 to 1000 MHz)
- Internally matched for ease of use.

APPLICATIONS

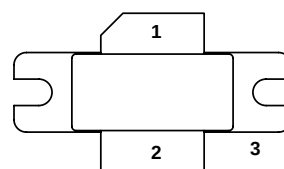
- RF power amplifier for GSM, EDGE and CDMA base stations and multicarrier applications in the 800 to 1000 MHz frequency range.

DESCRIPTION

125 W LDMOS power transistor for base station applications at frequencies from 800 MHz to 1000 MHz.

PINNING - SOT502A

PIN	DESCRIPTION
1	drain
2	gate
3	source; connected to flange



Top view

MBK394

Fig.1 Simplified outline SOT502A .

QUICK REFERENCE DATA

Typical RF performance at $T_h = 25$ °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dBc)	ACPR 400 (dBc)	EVM % rms (AV)
2-tone	920	125 (PEP)	15.5	37	-32	–	–
1-tone CW		125	16.5	54	–	–	–
GSM EDGE		45 (AV)	15	32	–	-64	2

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	75	V
V_{GS}	gate-source voltage	–	±15	V
T_{stg}	storage temperature	-65	150	°C
T_j	junction temperature	–	200	°C

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-c}$	thermal resistance from junction to case	$T_h = 25\ ^\circ\text{C}$, $P_L = 35\ \text{W}$ (AV), note 1	0.42	K/W
$R_{th\ j-h}$	thermal resistance from junction to heatsink	$T_h = 25\ ^\circ\text{C}$, $P_L = 35\ \text{W}$ (AV), note 2	0.62	K/W

Notes

1. Thermal resistance is determined under RF operating conditions.
2. Depending on mounting condition in application.

CHARACTERISTICS

$T_j = 25\ ^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 3\ \text{mA}$	75	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = 10\ \text{V}$; $I_D = 300\ \text{mA}$	4	–	5	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 36\ \text{V}$	–	–	3	μA
I_{DSX}	on-state drain current	$V_{GS} = V_{GSth} + 9\ \text{V}$; $V_{DS} = 10\ \text{V}$	45	–	–	A
I_{GSS}	gate leakage current	$V_{GS} = \pm 20\ \text{V}$; $V_{DS} = 0$	–	–	1	μA
g_{fs}	forward transconductance	$V_{DS} = 10\ \text{V}$; $I_D = 10\ \text{A}$	–	9	–	S
R_{DSon}	drain-source on-state resistance	$V_{GS} = 9\ \text{V}$; $I_D = 10\ \text{A}$	–	60	–	$\text{m}\Omega$

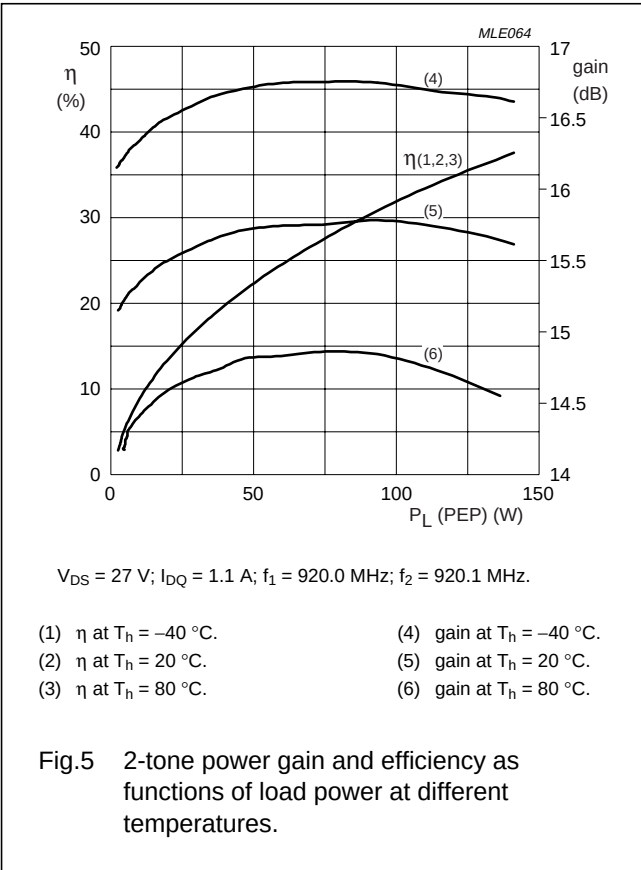
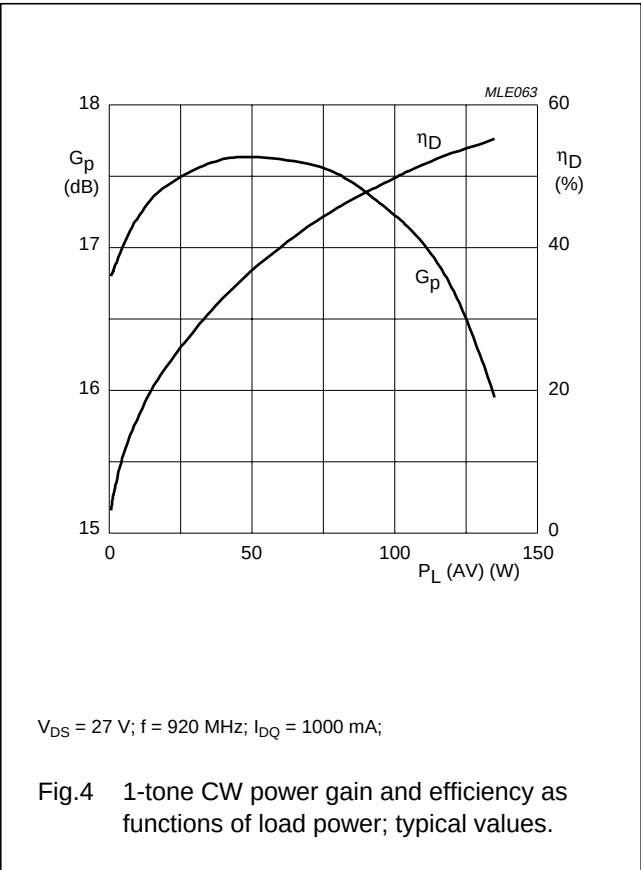
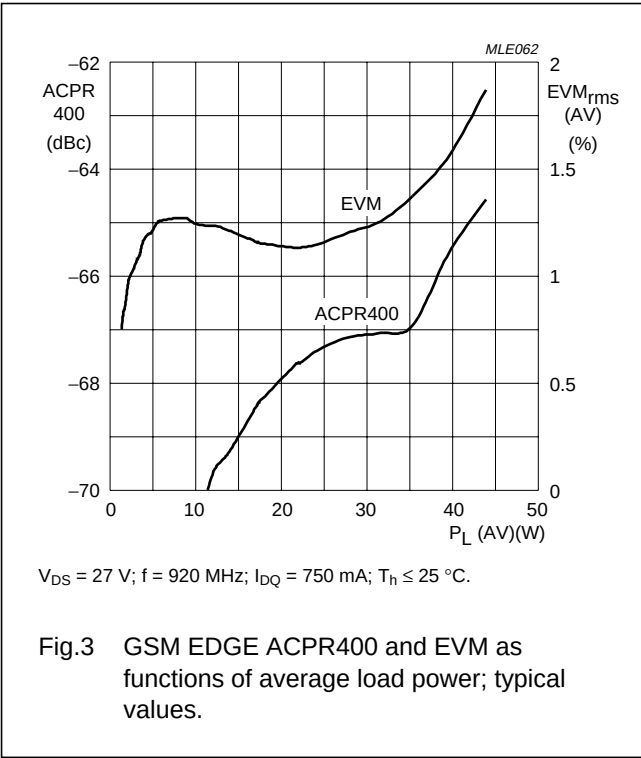
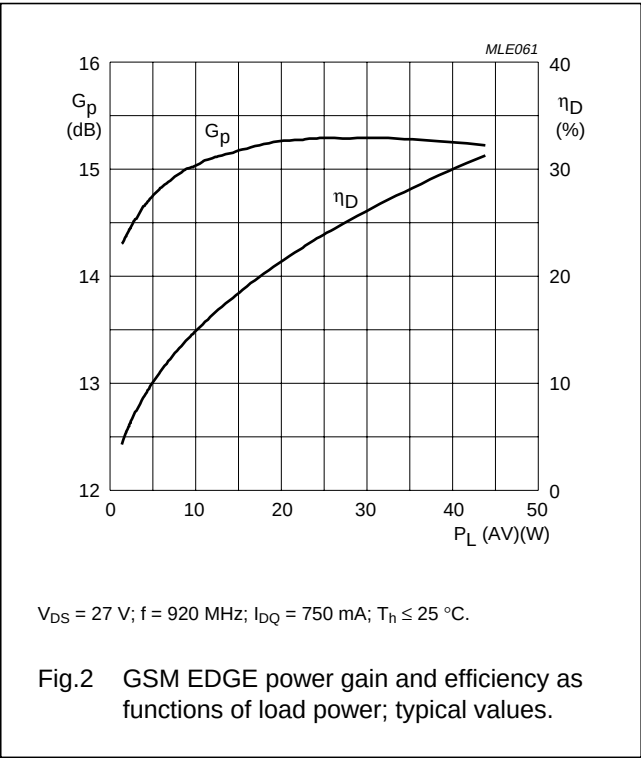
APPLICATION INFORMATION

RF performance in a common source class-AB circuit; $V_{DS} = 27\ \text{V}$; $T_h = 25\ ^\circ\text{C}$; unless otherwise specified.

Mode of operation: 2-tone CW, 100 kHz spacing; I _{DQ} = 1130 mA; f = 890 MHz						
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
G _p	gain power	P _L = 125 W (PEP)	14.6	15.5	–	dB
η _D	drain efficiency		33	37	–	%
IRL	input return loss		–	–12	–6	dB
d ₃	third order inter modulation distortion		–	–32	–25	dBc
Mode of operation: GSM EDGE; I _{DQ} = 750 mA; f = 920 MHz						
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
G _p	gain power	P _L = 45 W (AV)	–	15	–	dB
η _D	drain efficiency		–	32	–	%
ACPR 400	adjacent channel power ratio		–	–64	–	dBc
EVM (AV)	EVM rms average signal distortion		–	2	–	%
EVM peak	EVM rms peak signal distortion		–	2.2	–	%
Mode of operation: 1-tone CW; I _{DQ} = 1000 mA; f = 920 MHz						
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
G _p	gain power	P _L = P _{L 1 dB} = 125 W	–	16.5	–	dB
η _D	drain efficiency		–	54	–	%

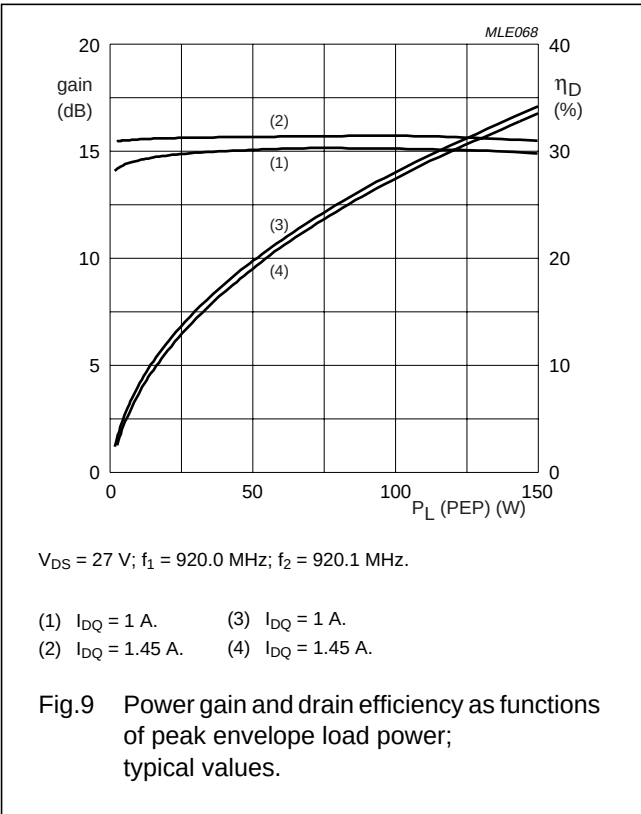
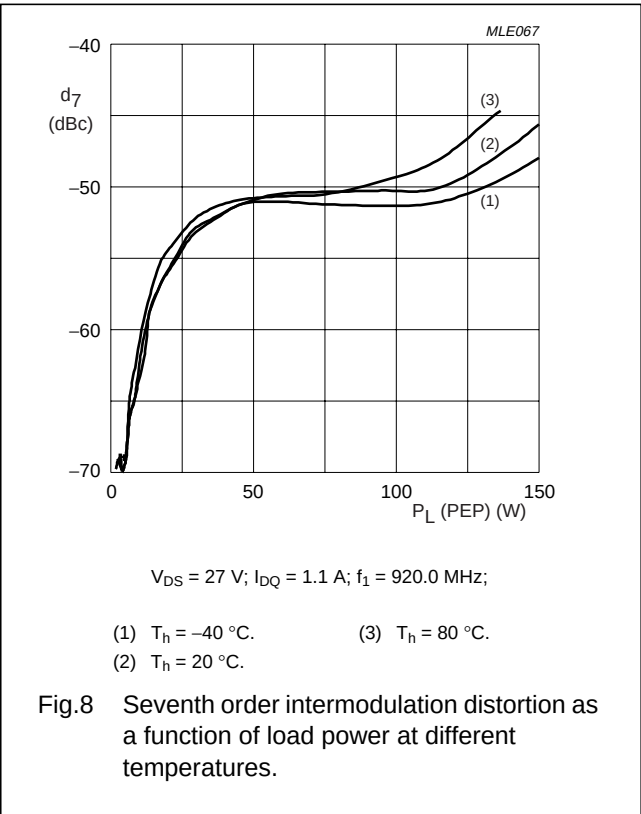
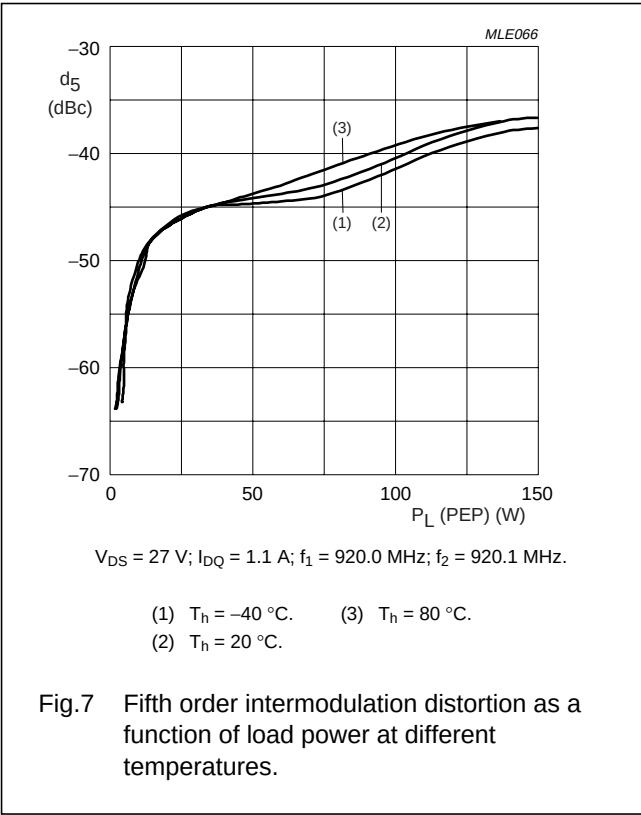
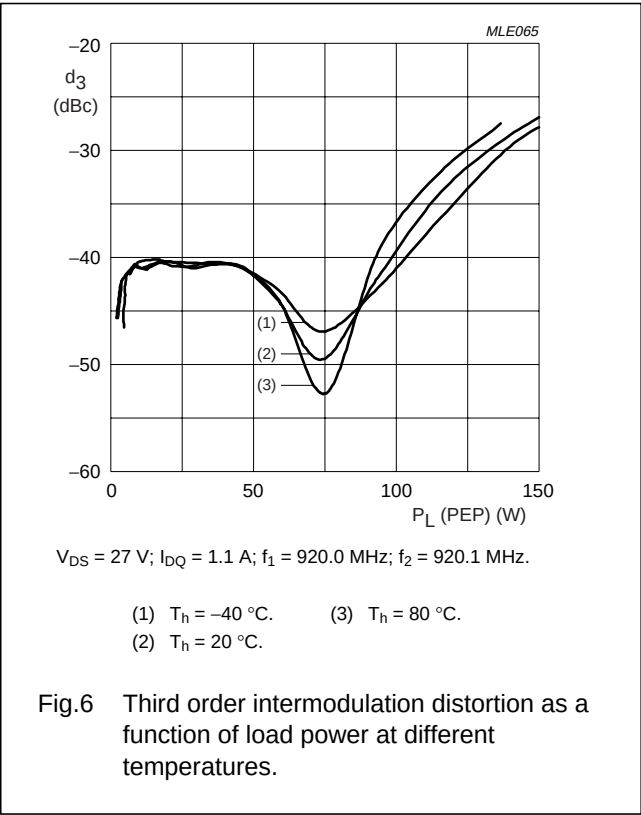
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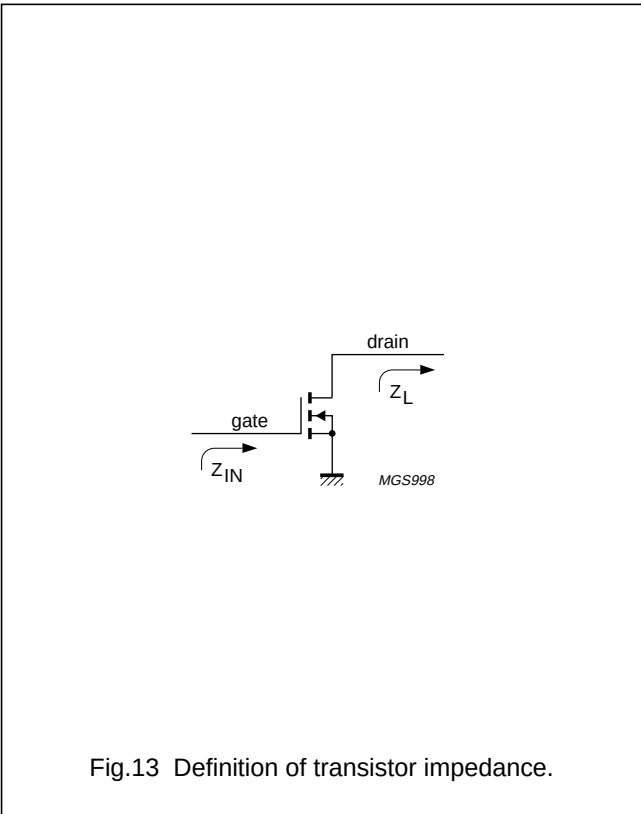
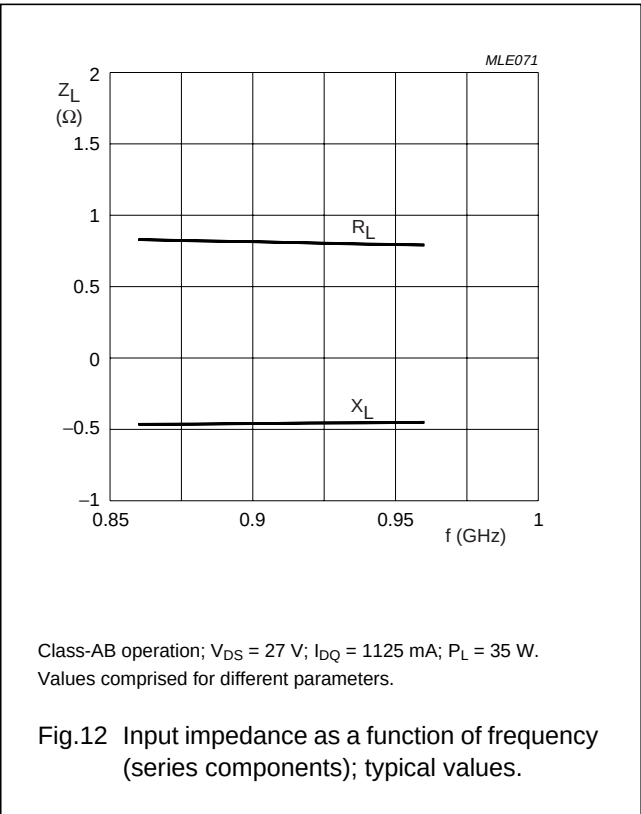
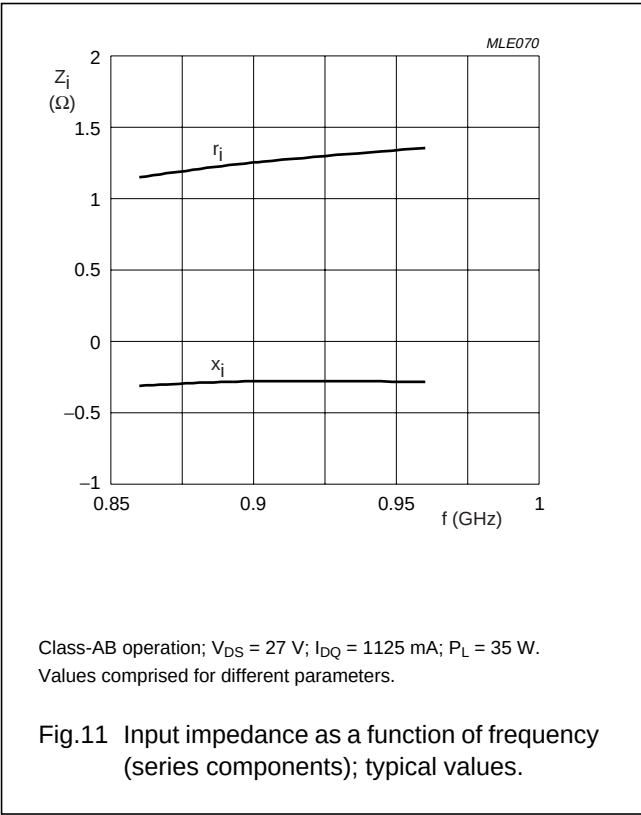
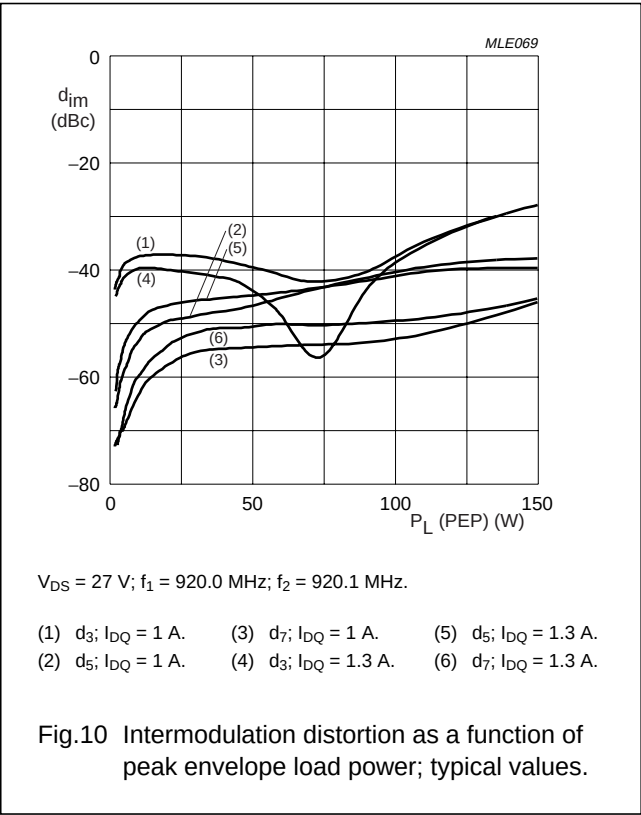
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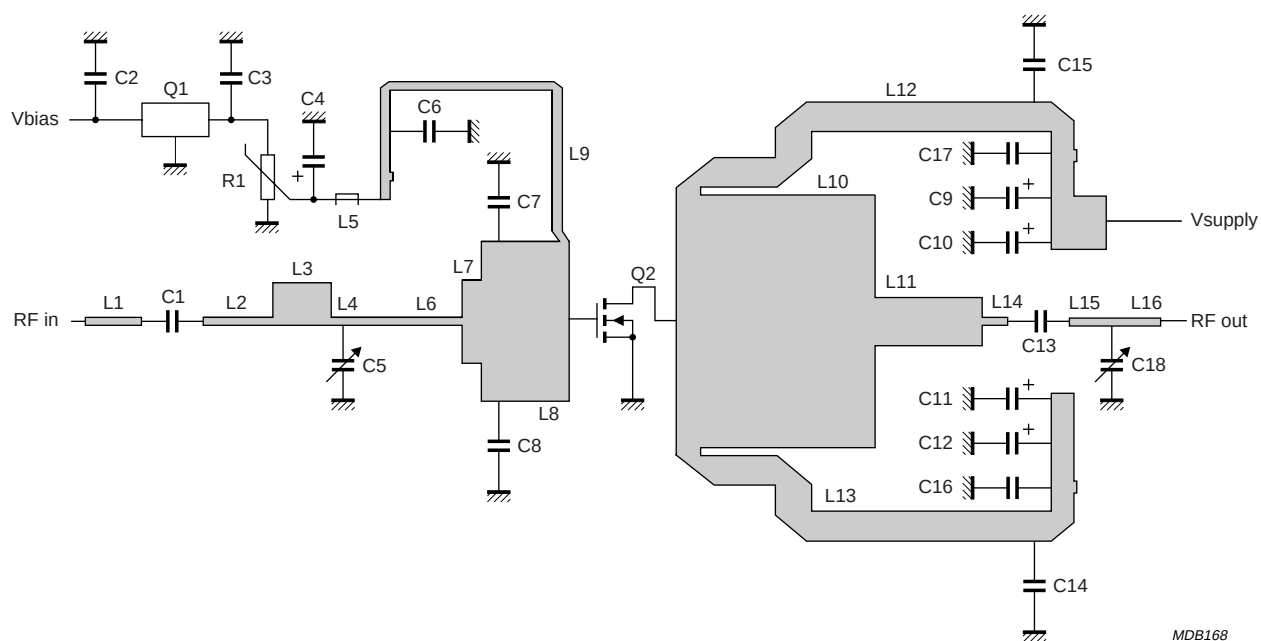
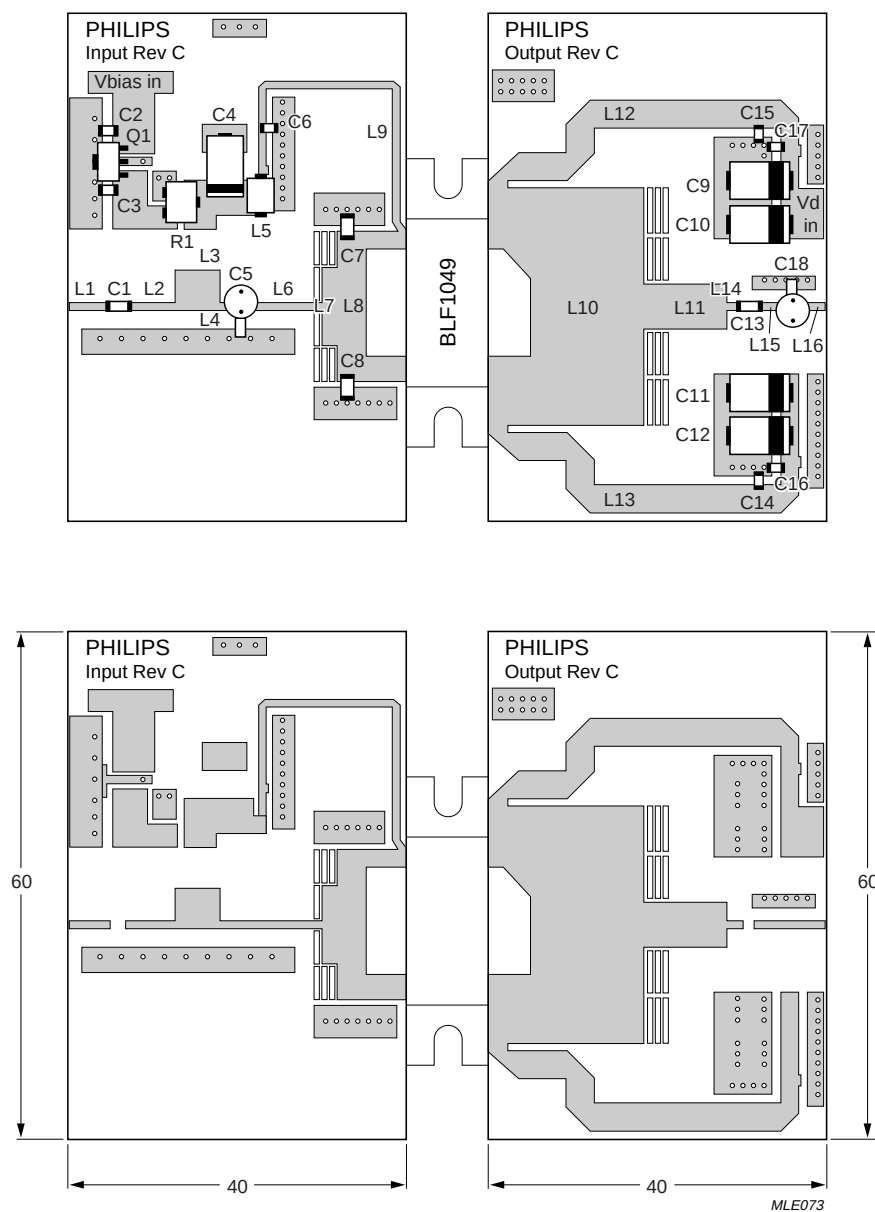


Fig.14 Test circuit for 860 to 900 MHz.

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Dimensions in mm.

The components are situated on one side of the copper-clad Rogers 6006 printed-circuit board ($\epsilon_r = 6.15$); thickness = 25 mm. The other side is unetched and serves as a ground plane.

Fig.15 Component layout for 860 to 900 MHz test circuit.

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List of components (see Figs 14 and 15)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
C1, C6, C13, C14, C15, C16, C17	multilayer ceramic chip capacitor; note 1	68 pF	
C2	multilayer ceramic chip capacitor; note 1	330 nF	
C3	multilayer ceramic chip capacitor; note 1	100 nF	
C4, C9, C10, C11, C12	tantalum capacitor	10 μ F	
C5, C18	air trimmer capacitor	5 pF	
C7, C8	multilayer ceramic chip capacitor	8.2 pF	
R1	potentiometer	1 k Ω	
Q1	7808 voltage regulator		
Q2	BLF1049 LDMOS transistor		
L1	stripline; note 2		5.22 $\times$ 0.92 mm
L2	stripline; note 2		6.47 $\times$ 0.92 mm
L3	stripline; note 2		5.38 $\times$ 4.8 mm
L4	stripline; note 2		2.4 $\times$ 0.92 mm
L5	ferroxcube		
L6	stripline; note 2		9.73 $\times$ 0.92 mm
L7	stripline; note 2		1.82 $\times$ 9.3 mm
L8	stripline; note 2		8.15 $\times$ 17.9 mm
L9	stripline; note 2		44 $\times$ 0.92 mm
L10	stripline; note 2		18.45 $\times$ 28.3 mm
L11	stripline; note 2		9.95 $\times$ 5.38 mm
L12, L13	stripline; note 2		37.6 $\times$ 3.35 mm
L14	stripline; note 2		2.36 $\times$ 0.92 mm
L15, L16	stripline; note 2		4.22 $\times$ 0.92 mm

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. The striplines are on a double copper-clad Rogers 6006 printed-circuit board ($\epsilon_r = 6.15$); thickness = 0.64 mm.

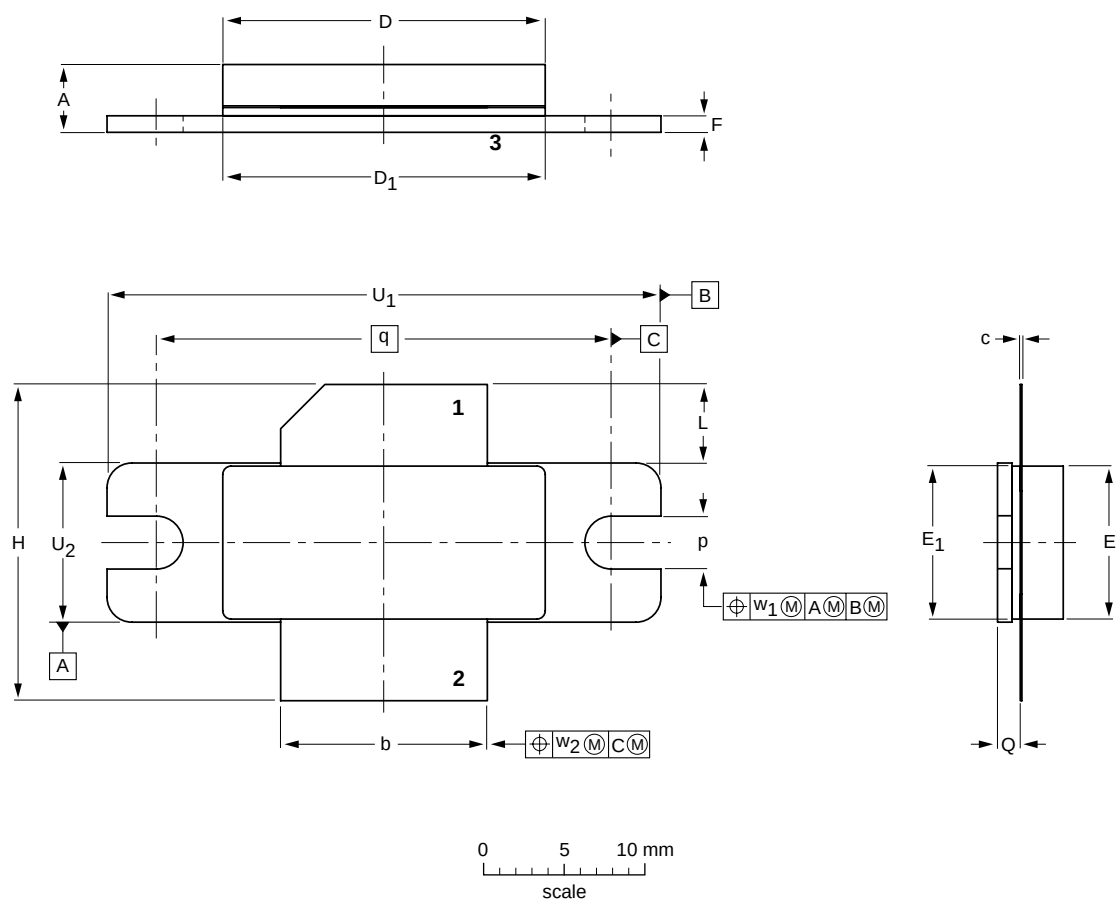
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PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	p	Q	q	U ₁	U ₂	w ₁	w ₂
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~99-12-28~~ 03-01-10

Base station LDMOS transistor

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